In the Claims:

1. (Currently Amended) An electronic device, having a first surface and a second surface formed in a single substrate, said device comprising:

a plurality of circuit elements formed in said [[a]] first surface of said single substrate, said plurality of circuit elements including at least one active circuit element and at least one redundant circuit element;

at least one programmable fuse element formed in said [[a]] second surface of said single substrate, said programmable fuse element storing, when said at least one active circuit element is defective, an indication thereof; and

at least one interconnect connecting said plurality of circuit elements and said programmable fuse element.

2. (Currently Amended) The device of claim 1 further comprising at least one opening formed in said single substrate and extending between said first surface and said second surface; said interconnect passing through said opening.

3. (Original) The device of claim 1 further comprising a plurality of programmable fuse elements formed in said second surface of said substrate.

4. (Currently Amended) The device of claim 3 [[4]] wherein said plurality of programmable fuses stores, when said at least one active circuit element is defective, an address thereof.

5. (Original) The device of claim 1 wherein said at least one programmable fuse element includes a two-dimensional array of programmable fuse elements and a plurality of leads arranged as rows and columns of a grid, each of said leads being connected to said front surface of said substrate by a respective interconnect, each of said programmable fuse elements providing a respective connection between a particular column lead and a particular row lead.

6. (Original) The device of claim 5 wherein values stored in a row of said array of programmable fuse elements are read by sequentially activating each column lead and reading an output on a respective row lead connected to said row of said array of programmable fuse elements.

7. (Currently Amended) The device of claim 1 wherein said at least one ~~plurality of~~ active circuit element comprises ~~elements includes~~ a plurality of memory cells, and said at least one redundant circuit element is a redundant memory cell.

8. (Currently Amended) ~~An memory~~ The electronic device of claim 1 wherein said ~~formed in a substrate, said device comprising:~~ [[a]] plurality of circuit elements formed in said [[a]] first surface of said single substrate~~, said plurality of circuit elements including~~ comprises a plurality of active memory cells and a plurality of redundant memory cells wherein said at least one programmable fuse element comprises[[;]] a plurality of programmable fuse elements formed in said [[a]] second surface of said single substrate; said plurality of programmable fuse elements storing, when said at least one of said plurality of active memory cells is defective, an address

thereof; and wherein said at least one internet comprises a plurality of interconnects connecting said plurality of circuit elements and said programmable fuse elements.

9. (Currently Amended) The device of claim 8 further comprising a plurality of openings formed in said single substrate and extending between said first surface and said second surface; a respective one of said plurality of interconnects passing through a respective one of said plurality of openings.

10. (Currently Amended) The device of claim 8 wherein said plurality of programmable fuse elements is arranged as a two-dimensional array of programmable fuse elements, and said device further comprises a plurality of leads arranged as rows and columns of a grid, each of said leads being connected to said first ~~front~~ surface of said substrate by a respective one of said plurality of interconnects, each of said programmable fuse elements providing a respective connection from a particular column lead to a particular row lead.

11. (Original) The device of claim 10 wherein values stored in a row of said array of programmable fuse elements are read by sequentially activating each column lead and reading an output on a respective row lead connected to said row of said array of programmable fuse elements.

12. (Currently Amended) An electronic device having a first surface and a second surface formed in a single substrate, said device comprising:

a plurality of circuit elements formed in said [[a]] first surface of said single substrate;

at least one bonding pad formed in a second surface of said substrate; and

at least one interconnect connecting said plurality of active circuit elements and said at least one bonding pad.

13. (Currently Amended) The device of claim 12 further comprising at least one opening formed in said substrate and extending between said first surface and said second surface; said interconnect passing through said at least one opening.

14. (Original) The device of claim 12 wherein said plurality of circuit elements includes a plurality of memory cells.

15. (New) An electronic chip having a first surface and a second surface formed on a single semiconductor substrate, said electronic chip comprising:

a plurality of circuit elements formed on said first surface of said single semiconductor substrate, said plurality of circuit elements including at least one active circuit element and at least one redundant circuit element;

at least one programmable fuse element formed on said second surface of said single semiconductor substrate, said programmable fuse element storing an indication that said at least one active circuit element is defective;

at least one opening formed in said single semiconductor substrate and extending between said first surface and said second surface; and

at least one interconnect passing through said at least one opening connecting said plurality of circuit elements and said programmable fuse element.

16. (New) The device of claim 15 wherein said at least one programmable fuse element comprises a plurality of programmable fuse elements.

17. (New) The device of claim 15 wherein said at least one programmable fuse element comprises a two-dimensional array of programmable fuse elements and a plurality of leads arranged as rows and columns of a grid, each of said leads being connected to said first surface of said single semiconductor substrate by a respective interconnect, each of said programmable fuse elements providing a respective connection between a particular column lead and a particular row lead.

18. (New) The device of claim 16 wherein said plurality of circuit elements comprises a plurality of active circuit elements, and a plurality of redundant circuit elements.

19. (New) The device of claim 18 wherein said plurality of active circuit elements comprises a plurality of memory cells and wherein said plurality of redundant circuit elements comprises a plurality of redundant memory cells.